ABSTRACT OF THE DISCLOSURE

A debugging apparatus includes: a processor core operated by a program stored in a program memory to read a data stored in a data memory or write a data; a debugger controller for performing a debugging on the processor core upon receipt of a command from a host computer and outputting a data break point address; and a memory break controller for observing an address of a data memory used by the processor core, recognizing an address as a break point address to output a break signal to the debugger controller and the processor core to suspend the operation of the processor core, when the address is sensed to be identical, and transmitting a corresponding address and data to the host computer through the debugger controller. Since an address and a data of a specific data memory are monitored to recognize a data flow and change of the specific address, an error that an erroneous calculation is inputted a during processing or a data memory is erroneously assigned is quickly sensed. Thus, a time and an expense for a debugging operation can be much saved. In addition, by adding a data debugging method to the conventional program debugging method, a program development environment is set similar to an environment substantially operated by the processor. Thus, a time and an expense for developing a program can be also saved.